REMARKS/ARGUMENTS

1. Claims 1-9 are pending in the application.

2. Claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,805,931 ("*Morzano, et al.*") in view of U.S. Patent No. 5,367,646 ("*Pardillos, et al.*"). Applicant respectfully traverses this rejection.

Before discussing the rejection, it would be useful to review Applicant's invention, as claimed. Applicant's invention, as claimed relates to a memory device which interfaces with an integrated circuit communicating via a communication bus. An illustrative example of the device is shown in the application in Figure 4. As recited in claim 1, the memory device communicates via a communication bus which is shown as bus 30 in the drawing. The device comprises a decoding circuit which is shown as the decoder 80 in Figure 4 which receives the communication signals via the communication bus 30. The decoder 80 decodes the communication signals and generates a plurality of protocol signals in response thereto. The protocol signals are supplied to the protocol select circuits 66. As stated in claim 1, the memory device further comprises a protocol select circuit for receiving said plurality protocol signals. Thus, as shown in Figure 4, the output of the decoder circuit 80 is connected to the protocol select circuit 66. Claim 1 further recites an array of memory cells. This is not shown in Figure 4 but is shown as the memory 50 in Figure 3. Claim 1 further recites a controller circuit for controlling the operation of the array of memory cells. In Figure 4, the controller circuit is the finite state machine circuit 70. Finally, the protocol select circuit which is shown as 66 in the drawing, configures the controller circuit or the FSM 70 in response to the plurality protocol signals received from the decoder circuit 80. Thus, claim 1 as recited discloses a decoder circuit 80 connected to the communication bus 30 for receiving communication signals therefrom, and generates signals that are supplied to the protocol select circuit 66 which processes those signals and supplies them to the finite state machine circuit 70, which then controls the memory array 50.

Turning to the rejection, the Examiner asserted that as to claim 1 *Morzano, et al.* teaches a decoding circuit shown as item 378 in Figure 10. The Examiner further alleged that a

protocol select circuit for receiving said plurality protocol signals is shown in *Moranzo, et al.* at column 14, lines 8-23 by the "controller circuit." Column 14, lines 8-23 refers to the drawing shown in Figure 14 and the controller circuits are the controller circuits 562, 564. . .570 (see column 14, line 20). According to the Examiner, the protocol select circuit or the controller circuit shown as 562, 564, etc. must receive the protocol signals. However, as discussed hereinabove, claim 1 recites that the protocol signals are generated by the decoding circuit. In this case, the Examiner has failed to show that the controller circuits 562, 564. . .570 shown in Figure 14 of *Morzano, et al.* receives the signals from the decoder 378 shown in Figure 10 of *Morzano, et al.* In fact, a review of Figure 14 of *Morzano, et al.* shows that the control circuit 562 generates signals which are supplied to the decoder 542, rather than receiving signals that are the outputs of the decoder. Accordingly, for at least this reason, Applicant respectfully submits that the Examiner has not shown how claim 1 is met by *Morzano, et al.*

The Examiner also asserted that an array of memory cells is disclosed in *Morzano, et al.* by the SAMs, as disclosed in column 14, lines 8-23. Finally, the Examiner asserted that the protocol select circuit which configures the controller circuit is disclosed in Figures 7-13 and column 14, lines 8-23 of *Morzano, et al.*. Applicant respectfully traverses this characterization of *Morzano, et al.*

As previously discussed, as set forth in claim 1, the array of memory cells is controlled by the controller circuit with the controller circuit being configured by the protocol select circuit. According to the Examiner, the protocol select circuit of claim 1 is met by the controller circuit of *Morzano, et al.* which is elements 562, 564 and 570. Yet, no disclosure is shown by the Examiner of where the protocol select circuits are disclosed in *Morzano, et al.* A review of Figures 7-13 show that they are all similar to Figure 10 in that the circuit shown is connected to receive the signals from the SAM bus, shown as 52 in Figure 3 and to generate decode signals (see Figure 13). Therefore, Applicant respectfully submits that *Morzano, et al.* fails to show the protocol select circuit which receives the decode signals and configure the controller circuit.

The Examiner acknowledged that *Morzano, et al.* does not disclose a control circuit for controlling the operation of the array of memory cells. However, according to the

examiner, this missing element is taught by *Pardillos, et al.* which shows a memory access controller disclosed in column 21, line 50-column 22, line 29. Even if it were obvious to combine *Pardillos, et al.* with *Morzano, et al.*, an assumption not conceded by Applicant, the Examiner still has not shown how the control circuit can be configured by the protocol select circuit "in response to the plurality of protocol signals" as set forth in claim 1. Thus, even if it were obvious to combine *Pardillos, et al.* and *Morzano, et al.*, an assumption not conceded by Applicant, the resulting combination would still not yield Applicant's invention as claimed in claim 1. Therefore, Applicant respectfully submits that the rejection of claim 1 is an error.

3. Claims 2-8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Morzano, et al.* in view of *Pardillos, et al.* and further in view of U.S. Patent No. 6,542,391 ("*Pereira, et al.*"). Applicant respectfully traverses this rejection. With respect to claims 2-6, which depend upon claim 1, for at least the reasons described heretofore with regard to the inadequacy of the combination of *Pardillos, et al.* and *Morzano, et al.*, the combination of *Pardillos, et al.* and *Morzano, et al.* and *Pereira, et al.* would not yield Applicant's invention, as claimed.

Further, in rejecting claims 2-6, the Examiner conceded that neither *Morzano, et al.* nor *Pardillos, et al.* teaches a non-volatile storage element and volatile storage element is a register, flip-flop and SRAM. However, according to the Examiner, *Pereira* teaches a non-volatile storage element and volatile storage element as a register, flip-flop and SRAM in column 18, lines 17-25; column 9, lines 4-27. This rejection is hereby traversed.

With respect to claim 3 at least, the claim recites the protocol select circuit is a volatile storage element. As previously discussed, *Morzano* and *Pardillos* even if combined, does not disclose a protocol select circuit to configure the controller circuit in response to the plurality protocol signals. Further, there is no disclosure in *Morzano* or *Pardillos* or *Pereira* that a protocol select circuit can be a volatile storage element. Lastly, none of the three cited references teaches that protocol select circuit can be a register, flip-flop, or SRAM. Therefore, for these reasons, Applicant respectfully submit that claims 2-6 are patentable over the combination *Morzano, Pardillos* and *Pereira*.

With respect to claim 7, it is similar in scope to claim 1 except it is more limited to the communication bus as an LPC bus having a start field. Thus Applicant's arguments with regard to the inapplicability of *Morzano* and *Pardillos* as applied to claim 1 also applies with regard to the rejection of *Morzano* and *Pardillos* as applied to claim 7. The addition of the reference Pereira, does not overcome this shortcoming. Therefore, Applicant respectfully submits that the combination *Morzano*, *Pardillos*, and *Pereira* still would not result in Applicant's invention, as claimed in claim 7.

4. As for claims 8 and 9, each of which is a dependent claim depending upon claim 7, for the same reasons discussed with regard to the inadequacy of the combination *Morzano*, *Pardillos*, and *Pereira*, the combinations of these references would still not disclose all of the combined elements of claims 8 and 9. Therefore, for this reason, Applicant's submit that claims 8 and 9 are patentable over the combination *Morzano*, *Pardillos*, and *Pereira*.

5. With respect to claim 9, this claim has been rejected on the basis of Morzano, *Pardillos*, and *Pereira* and U.S. Patent No. 6,188,602 ("*Alexander*").

For the same reasons discussed with regard to the inadequacy of rejection of claim 8, Applicant's respectfully submit that the combination *Morzano*, *Pardillos*, and *Pereira*, does not anticipate all of the element of claim 7 and since claim 9 is dependent upon claim 7, the addition of the reference *Alexander* still would not yield Applicant's invention, as claimed in claim 9.

Therefore, for all of these reasons, Applicant respectfully request reconsideration of the claims.

The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 07-1896, **referencing docket number 351913-992800**.

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Respectfully submitted,

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